What is claimed is:

1. A ferroelectric random access memory (FeRAM) device, comprising:

a plurality of memory cells arranged in an M × J matrix, wherein M is a positive integer more than three and J is a positive integer;

a number of reference cells connected to each column of the memory cells; and

a cell selection means for selecting a memory cell in response to address signals from an external circuit and selecting a reference cell corresponding to the selected memory cell.

2. The FeRAM device as recited in claim 1, wherein the number of memory cells of each column is $M = 2^N$ and the number of reference cells is N.

3. The FeRAM device as recited in claim 1, wherein said cell selection means includes:

a memory cell selection circuit connected to the memory cells via word lines for generating a memory cell selection signal in response to the address signals to select a corresponding memory cell; and

a reference cell selection circuit connected to the reference cells via reference word lines for generating a reference cell selection signal to select the corresponding reference cell.

4. The FeRAM device as recited in claim 3, wherein said memory

cell selection circuit includes:

a plurality of NAND gates, each NAND gate for receiving address signals from an external circuit to perform NAND logical operation; and

a plurality of inverters, each inverter for inverting an output signal of each NAND gate to generate the memory cell selection signal.

4. The FeRAM device as recited in claim 2, wherein said reference cell selection circuit includes:

a plurality of NAND gates, each NAND gate for receiving address signals from an external circuit to perform NAND logical operation; and

a plurality of inverters, each inverter for inverting an output signal of each NAND gate to generate the reference cell selection signal.

5. The FeRAM device as recited in claim 1, wherein the number of the memory cells is 2^8 and the number of the reference cells is eight.

6. The FeRAM device as recited in claim 3, wherein each NAND gate of said memory cell selection circuit has eight input terminals.

7. The FeRAM device as recited in claim 4, wherein each NAND gate of said reference cell selection circuit has three input

terminals.

9. The FeRAM device as recited in claim 1, wherein said memory cells have one transistor and one ferroelectric capacitor, respectively.

10. The FeRAM device as recited in claim 1, wherein said reference cells have one transistor and one ferroelectric capacitor, respectively.

11. The FeRAM device as recited in claim 1, wherein said memory cells are connected to first bit line.

12. The FeRAM device as recited in claim 11, wherein said reference cells are connected to second bit line.

13. The FeRAM device as recited in claim 12, wherein said memory cells and said reference cells shares a cell plate, wherein the cell plate is positioned between the first bit line and the second bit line.